

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit: 2183
Serial No.: 10/069,306 Examiner: Daniel H. Pan
Filed : July 3, 2002
Assignee : Intel Corporation
Title : INSTRUCTION FOR MULTITHREADED PARALLEL PROCESSOR

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Kindly accept this Information Disclosure Statement under Rule 97(c)(2). Please apply the rule 17(p) certification fee in the amount of \$180 to deposit account 06-1050.

Respectfully submitted,

Date: February 23, 2007

/Scott C Harris/
Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
USPTO Customer No. **20985**
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-303US1	Application No. 10/069,306
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	
		Filing Date July 3, 2002	Group Art Unit 2183

(37 CFR §1.98(b))

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0038403	03/2002	Wolrich et al.			
	AB	3,577,189	05/1971	Cocke et al.			
	AC	3,881,173	04/1975	Larsen et al.			
	AD	4,454,595	06/1984	Cage			
	AE	4,471,426	09/1984	McDonough			
	AF	4,477,872	10/1984	Losq et al.			
	AG	4,569,016	02/1986	Hao et al.			
	AH	4,742,451	05/1988	Bruckert et al.			
	AI	4,755,966	07/1988	Lee et al.			
	AJ	4,808,988	02/1989	Burke et al.			
	AK	4,816,913	03/1989	Harney et al.			
	AL	4,847,755	07/1989	Morrison et al.			
	AM	4,992,934	02/1991	Portanova et al.			
	AN	5,045,995	09/1991	Levinthal et al.			
	AO	5,056,015	10/1991	Baldwin et al.			
	AP	5,165,025	11/1992	Lass			
	AQ	5,170,484	12/1992	Grondalski			
	AR	5,187,800	02/1993	Sutherland			
	AS	5,189,636	02/1993	Patti et al.			
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	AU	5,274,770	12/1993	Khim Yeoh et al.			
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	AW	5,450,603	09/1995	Davies			
	AX	5,463,746	10/1995	Brodnax et al.			
	AY	5,509,130	04/1996	Traubert et al.			
	AZ	5,544,337	08/1996	Beard et al.			
	BA	5,572,690	11/1996	Molnar et al.			

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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	BC	5,640,538	06/1997	Dyer et al.			
	BD	5,669,012	09/1997	Shimizu et al.			
	BE	5,680,564	10/1997	Divivier et al.			
	BF	5,701,435	12/1997	Chi			
	BG	5,724,563	03/1998	Hasegawa			
	BH	5,748,950	05/1998	White et al.			
	BI	5,802,373	09/1998	Yates et al.			
	BJ	5,812,811	09/1998	Dubey et al.			
	BK	5,815,698	09/1998	Holmann et al.			
	BL	5,815,714	09/1998	Shridhar et al.			
	BM	5,819,080	10/1998	Dutton et al.			
	BN	5,832,258	11/1998	Kiuchi et al.			
	BO	5,838,975	11/1998	Abramson et al.			
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	BS	5,875,470	02/1999	Dreibelbis et al.			
	BT	5,898,866	04/1999	Atkins et al.			
	BU	5,900,025	05/1999	Sollars			
	BV	5,923,872	07/1999	Chrysos et al.			
	BW	5,928,358	07/1999	Takayama et al.			
	BX	5,937,177	08/1999	Molnar et al.			
	BY	5,943,491	08/1999	Sutherland et al.			
	BZ	5,944,816	08/1999	Dutton et al.			
	CA	5,946,222	08/1999	Redford			
	CB	5,956,514	09/1999	Wen et al.			

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	CC	5,993,627	11/1999	Anderson et al.			
	CD	6,009,505	12/1999	Thayer et al.			
	CE	6,061,710	05/2000	Eickemeyer et al.			
	CF	6,139,199	10/2000	Rodriguez			
	CG	6,141,348	10/2000	Muntz			
	CH	6,145,123	11/2000	Torrey et al.			
	CI	6,157,988	12/2000	Dowling			
	CJ	6,195,739	02/2001	Wright et al.			
	CK	6,205,468	03/2001	Diepstraten et al.			
	CL	6,223,208	04/2001	Kiefer et al.			
	CM	6,223,277	04/2001	Karguth			
	CN	6,230,119	05/2001	Mitchell			
	CO	6,230,230	05/2001	Joy et al.			
	CP	6,230,261	05/2001	Henry et al.			
	CQ	6,259,699	07/2001	Opalka et al.			
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	CT	6,279,066	08/2001	Velingker			
	CU	6,314,510	11/2001	Saulsbury et al.			
	CV	6,338,133	01/2002	Schroter			
	CW	6,378,124	04/2002	Bates et al.			
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	CY	6,385,720	05/2002	Tanaka et al.			
	CZ	6,401,155	06/2002	Saville et al.			
	DA	6,408,325	06/2002	Shaylor			
	DB	6,446,190	09/2002	Barry et al.			
	DC	6,496,847	12/2002	Bugnon et al.			

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	DE	6,543,049	04/2003	Bates et al.			
	DF	6,560,629	05/2003	Harris			
	DG	6,560,671	05/2003	Samra et al.			
	DH	6,564,316	05/2003	Perets et al.			
	DI	6,574,702	06/2003	Khanna et al.			
	DJ	6,697,935	02/2004	Borkenhagen et al.			
	DK	6,862,676	03/2005	Knapp et al.			
	DL	6,976,095	12/2005	Wolrich et al.			
	DM	6,983,350	01/2006	Adiletta et al.			
	DN	7,020,871	03/2006	Bernstein et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	DO	0 130 381	01/1985	Europe				
	DP	0 463 855	01/1992	Europe				
	DQ	0 476 628	03/1992	Europe				
	DR	0 696 772	02/1996	Europe				
	DS	WO03/019399	03/2003	WIPO				
	DT	WO03/085517	10/2003	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	DU	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
	DV	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: http://www.romilly.co.uk/whathart.htm >
	DW	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", <i>IEEE</i> , pp. 57-62, (1996).

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Other Documents (include Author, Title, Date, and Place of Publication)

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	DX	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
	DY	Hearing et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
	DZ	Hearing et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
	EA	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
	EB	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM & IEEE-CS</i> , 20(2):136-145, May 1992.
	EC	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
	ED	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).
	EE	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , IEEE, pp. 26-31 (1996).
	EF	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	EG	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	EH	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
	EI	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).
	EJ	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
	EK	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27th Annual Hawaiian International Conference on System Sciences</i> , IEEE, pp. 584-593, (1994).
	EL	Qammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	EM	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
	EN	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
	EO	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
	EP	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

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